Remarks

Claims 1, 2, and 4-23 are pending in this application. Claim 3 has been cancelled herein. Claims 1, 5, 12, 17, and 21 have been amended. The Examiner has rejected claims 1-23 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 7,017,054 to Schuckle et al, (hereinafter "Schuckle").

1. Rejections under 35 U.S.C. 102(e)

The Examiner has rejected claims 1-23 as being anticipated by Schuckle. A prior art patent, publication or event is for the same "invention," as that word is used in §102, and therefore anticipating, if the prior art patent, publication or event discloses each and every limitation found in the claims, either expressly or inherently. Rockwell Intern. Corp. v. U.S., 147 F.3d 1358, 1363 (Fed. Cir. 1998); Electro Med. Sys. S.A. v. Cooper Life Sciences, 34 F.3d 1048, 1052 (Fed. Cir. 1994). Each claim limitation must be found in a single prior art reference; references cannot be combined under §102. Apple Computer, Inc. v. Articulate Systems, Inc., 234 F.3d 14, 20 (Fed. Cir. 2000). Omission of any claimed element, no matter how insubstantial, is grounds for traversing a rejection based on §102. Connell v. Sears, Roebuck & Co., 722 F.2d 1542 (Fed. Cir. 1983).

Schuckle fails to disclose each and every limitation found in independent claims 1, 5, 12, 17, and 21. Specifically, Schuckle does not teach the element of a buffer maintained in a **memory controller** (or memory controller hub) having addresses of **system memory** data modified during the period that the processor is in a low power state.

In the Response to Arguments section of the Final Office Action, the Examiner argues that a cache inherently contains a buffer for prefetch operations involving those memory locations for which the cache contains an index, citing to column 7, lines 1-3 of Schuckle.

(Office Action, p.7) However, the cited portion of Schuckle discusses snooping of a memory transaction involving a cache or tag RAM. Specifically, in the cited portion of Schuckle, a processor 110 monitors (or snoops) a memory transaction, comparing the memory address to an index of addresses of memory locations stored in the processor's cache RAM, the index being stored in the tag RAM. (Schuckle, col. 7, lines 1-3) Figure 1 of Schuckle clearly shows that the cache (which, the Examiner alleges, contains the buffer) 115 does not reside in a memory controller (which Schuckle equates to a north bridge 140). (Schuckle, col. 4, lines 44-45) In contrast, Figure 1 of the present invention clearly shows that write tracking buffer 26 resides on memory controller hub 18.

The Examiner also repeatedly states that Schuckle describes a process by which modified data addresses may be accessed while keeping a processor in a low power state, referring only to column 7, lines 23-31 of Schuckle. (Office Action, p.8) However, this statement by the Examiner fails to address the requirement of the claims that the buffer have addresses of **system memory** data modified during the period that the processor is in a low power state.

The cited portion of Schuckle discusses how a processor is enabled to stay in a lower power state by implementing the mirror tag method of reducing snoop traffic in the north bridge 140. (Schuckle, col. 7, lines 23-31) Schuckle does teach that a mirror (or exact copy) of the cache tag RAM is maintained in a memory controller, but Applicant would like to clarify to the Examiner that the cache tag RAM is ". . . simply a directory of the memory locations **in the cache**." (emphasis added, Schuckle, col. 9, line 65 - col. 10, line 3) That is, the mirror tag is **not** a buffer containing addresses of **system** memory data modified during the period that the processor is in a low power state. The mirror copy of the cache tag is created and maintained by

writing the **same cache tag** information (in certain embodiments of Schuckle) to the mirror copy location on the north bridge when the information is **written to the cache memory**. (Schuckle, col. 10, lines 5-10 and claim 1) That is, the mirror tag, at best, contains the addresses of data **modified in the cache**. In fact, Schuckle explicitly states, "In one embodiment, a status bit in the cache tag is set up to indicate whether the **cache line has been modified**." (Schuckle, col. 10, lines 47-48). Thus, it is clear that the mirror tag is not a buffer having addresses of **system** memory data modified during the period that the processor is in a low power state.

Because Schuckle does not teach all of the elements of the independent claims, Applicant respectfully requests that the rejection of independent claims 1, 5, 12, 17, and 21 be withdrawn and contend that these claims are in condition for allowance.

Dependent claims 2, 4, 6-11, 13-16, 18-20, and 22-23 will not be individually discussed herein because they stem from otherwise allowable base claims.

Conclusion

Applicant respectfully submits that pending claims 1, 2, and 4-23 of the present invention, as amended, are allowable. Applicant respectfully requests that the rejection of the pending claims be withdrawn and that these claims be passed to issuance.

Respectfully submitted,

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